

WHAT IS CLAIMED IS:

1 1. A pipelined data processor capable of predicated
2 instruction execution dependent upon the state of an
3 instruction designated predicate register comprising:
4 a data register file including a plurality of read/write,
5 general purpose data registers;
6 an instruction decode unit operative during an
7 instruction decode pipeline phase receiving fetched
8 instructions and determining the identity of at least one
9 source operand data register, a destination operand data
10 register and one of a plurality of functional units for
11 execution of each instruction, said instruction decode unit
12 further identifying a predicate register responsive to receipt
13 of a predicated instruction;
14 a plurality of functional units operative during an
15 execution pipeline phase connected to said instruction decode
16 unit for performing a data processing operation on at least
17 one source operand recalled from at least one corresponding
18 instruction designated source data register and producing a
19 result, said functional unit responsive to a predicate
20 instruction to write said result to an instruction designated
21 destination data register if said corresponding predicate data
22 register has a first state and to nullify said instruction and
23 not write said result if said predicate register has a second
24 state opposite to said first state;
25 a scoreboard bit corresponding to each data register
26 capable of serving as a predicate register, each scoreboard
27 bit connected to said instruction decode unit to be set to a
28 first digital state upon determining said corresponding data

29 register is a destination for an instruction and connected to
30 said plurality of functional units to be reset to a second
31 digital state opposite to said first digital state upon
32 functional unit write of a result to said corresponding data
33 register; and

34 each functional unit is further operative responsive to a
35 predicate instruction during a decode pipeline phase to
36 nullify said predicate instruction of a following execution
37 phase if said predicate register has said second state and
38 said corresponding scoreboard bit has said second state.

1 2. The pipelined data processor of claim 1, wherein:
2 said functional unit is further operative to reset said
3 scoreboard bit to said second digital state upon nullification
4 of said instruction designating a corresponding data register
5 as a destination operand data register.

1 3. The pipelined data processor of claim 1, wherein:
2 each functional unit is further operative to operate at a
3 reduced power state for any execution pipeline phase nullified
4 during said preceding instruction decode phase.

1 4. A method of operating a pipelined data processor
2 capable of predicated instruction execution dependent upon the
3 state of an instruction designated predicate register
4 comprising the steps of:

5 setting a scoreboard bit to a first digital state upon
6 determining a corresponding data register is a destination for
7 an instruction;

8 resetting a scoreboard bit to a second digital state
9 opposite to said first digital state upon a write of a result
10 to said corresponding data register;

11 performing a data processing operation on at least one
12 source operand recalled from at least one corresponding
13 instruction designated source data register and producing a
14 result in response to a predicate instruction designating a
15 corresponding predicate data register and writing said result
16 to an instruction designated destination data register if said
17 corresponding predicate data register has a first state;

18 nullifying a predicate instruction and not writing said
19 result to the instruction designated destination data register
20 if said corresponding predicate register has a second state
21 opposite to said first state;

22 nullifying a predicate instruction for a following
23 execution phase if said corresponding predicate register has
24 said second state and said corresponding scoreboard bit has
25 said second state during a prior decode phase.

1 5. The method of claim 4, further comprising the step
2 of:

3 resetting a scoreboard bit to a second digital state upon
4 nullification of said instruction designating said
5 corresponding data register as a destination operand data
6 register.

1 6. The method of claim 4, further comprising the step
2 of:

3 operating the functional unit at a reduced power state
4 for any execution pipeline phase nullified during said
5 preceding instruction decode phase.

1 7. The method of claim 4 further comprising the step
2 of:
3 scheduling a last write to a data register a
4 predetermined number of pipeline phases before an execution
5 phase of a predicate instruction designating said data
6 register as a predicate register.